## DETAILED ACTION

### *Specification*

The amendments filed 12/22/2006, 4/24/2007 and 05/01/2009 are objected to under 35 U.S.C. 132(a) because they introduce new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: In paragraph [0025], as amended on 12/22/2006, the amendment "such that the notched spacer is thinner along the surface of the substrate, as illustrated in FIG. I j," is a new matter.

Applicant is required to cancel the new matter in the reply to this Office Action.

### *Drawings*

The drawings are objected to, because amended figure 1j, filed on 6/24/2008 introduces new matter. For example, in figure 1j, spacer layers 132 having thinner regions along sides of the gate electrode and the gate dielectric is a new matter.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 16-19, 21-24 and 26-28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There is no support in the specification as filed, for the claimed limitations of a "notched spacer having a first thickness in an upper portion and a second less thickness less than the first thickness in a lower portion adjacent to a surface of the substrate", as

recited in claim 16, and for the claimed limitations of "wherein the etching partially removes the lower portion of the first lager thereby forming a notch in the notched spacer such that the notched spacer has a second thickness in a direction substantially orthogonal to the sidewall of the gate electrode along the surface of the substrate that is less than the first thickness", as recited in claim 24.

There is no support in the disclosure and in the drawings for the claimed limitations of "a lower portion of the first layer at the surface of the substrate and a lower portion of the at least one sidewall of the gate electrode is not covered by the mask", as recited in claim 17.

There is no support in the disclosure and in the drawings for the claimed limitations of "a lower portion of the first layer extending along a surface of the substrate and extending up a lower sidewall portion of the sidewall of the gate electrode is exposed", as recited in claim 24.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuegraf et al. (7,009,264) in view of Boissonnet et al. (7,015,105) and Nishinohara (6,911,705).

Regarding claims 16 and 23, Schuegraf et al. teach in figure 2D and related text a method of forming a semiconductor device, the method comprising:

forming a gate electrode 211 having sidewalls on a region in a substrate, the region in the substrate having a first conductivity type;

forming a notched spacer 221 alongside the gate electrode sidewalls, the notched spacer having a first thickness in an upper portion and a second less thickness less than the first thickness in a lower portion adjacent to a surface of the substrate thereby forming a notch in the lower portion of the notched spacer, the notched spacer comprising a single homogenous layer;

Schuegraf et al. do not teach performing a first ion implant at an oblique angle to the substrate so as to implant ions beneath the gate electrode wherein the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type.

Boissonnet et al. teach in figures 12 and 13 and related text performing a first ion implant 22 at an oblique angle to the substrate so as to implant ions beneath the gate electrode 51 wherein the gate electrode 51 and the notched spacer 181 act as masks during the first ion implant, the first ion implant using ions of the first conductivity type,

and performing one or more second ion implants using ions of a second conductivity type.

Nishinohara teach in figures 8 and 9 and related text (column 8, lines 52-63) performing a first ion implant at an oblique angle to the substrate so as to implant ions (halo region) beneath the gate electrode 4 wherein the gate electrode 4 and the spacer 20a act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to perform a first ion implant at an oblique angle to the substrate so as to implant ions beneath the gate electrode wherein the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type in Schuegraf et al.'s device in order to operate the device in its intended use by simplifying the processing steps of making the device by using the device in a CMOS application (which requires first and second conductivity types implantations), and in order to reduce short channel effects and to adjust the threshold voltage of the device, respectively.

Regarding claim 21, Schuegraf et al. do not state that the step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate.

Boissonnet et al. teach the step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate.
Nishinohara teaches the step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate, in order to obtain proper doping distribution.

Regarding claim 22, Schuegraf et al. do teach the notched spacer comprising silicon dioxide. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a notched spacer comprising silicon dioxide in prior art's device in order to simplify the processing steps of making the device by using conventional isolating material, of which official notice is taken.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuegraf et al., Boissonnet et al. and Nishinohara, as applied to claim 16 above, and further in view of Chen et al. (6,610,571).
Regarding claim 17, Schuegraf et al., Boissonnet et al. and Nishinohara teach substantially the entire claimed structure, as applied to claim 16 above, except teaching the method of forming the notched spacer.

Chen et al. teach in figures 2-4 and related text a method of forming a notched spacer comprises forming a first layer 50 and a second layer 52, forming a mask out of the second layer on the first layer, wherein an upper portion of the first layer 50 alongside an upper portion of at least one sidewall of the gate electrode 14 is covered by the mask(see figure 3), and wherein a lower portion of the first layer 50 at the surface of the substrate and a lower portion of the at least one sidewall of the gate electrode is not covered by the mask, isotropically etching the first layer such that the lower portion of the first layer is partially removed, and removing the mask (the portion of layer 52, as depicted in figure 4, which was used as a mask).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's notched spacer by forming a first layer and a second layer, forming a mask out of the second layer on the first layer, wherein an upper portion of the first layer alongside an upper portion of at least one sidewall of the gate electrode is covered by the mask, and wherein a lower portion of the first layer at the surface of the substrate and a lower portion of the at least one sidewall of the gate electrode is not covered by the mask, isotropically etching the first layer such that the lower portion of the first layer is partially removed, and removing the mask, in order to simplify the processing steps of making the device by using a conventional method.

Regarding claim 19, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a mask formed of silicon dioxide in prior art's

device in order to simplify the processing steps of making the device by using conventional isolating material, of which official notice is taken.

Claims 16 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al. (6,417,084) in view of Boissonnet et al. (7,015,105) and Nishinohara (6,911,705).

Regarding claims 16 and 22, Singh et al. teach in figures 6-11 and related text a method of forming a semiconductor device, the method comprising:

forming a gate electrode 70 having sidewalls on a region in a substrate, the region in the substrate 62 having a first conductivity type;

forming a notched spacer 74 alongside the gate electrode sidewalls, the notched spacer having a first thickness in an upper portion and a second less thickness less than the first thickness in a lower portion adjacent to a surface of the substrate thereby forming a notch in the lower portion of the notched spacer, the notched spacer comprising a single homogenous silicon dioxide layer;

Singh et al. do not teach performing a first ion implant at an oblique angle to the substrate so as to implant ions beneath the gate electrode wherein the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type.

Boissonnet et al. teach in figures 12 and 13 and related text performing a first ion implant 22 at an oblique angle to the substrate so as to implant ions beneath the gate

electrode 51 wherein the gate electrode 51 and the notched spacer 181 act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type.

Nishinohara teach in figures 8 and 9 and related text (column 8, lines 52-63) performing a first ion implant at an oblique angle to the substrate so as to implant ions (halo region) beneath the gate electrode 4 wherein the gate electrode 4 and the spacer 20a act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to perform a first ion implant at an oblique angle to the substrate so as to implant ions beneath the gate electrode wherein the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type in Singh et al.'s device in order to operate the device in its intended use by simplifying the processing steps of making the device by using the device in a CMOS application (which requires first and second conductivity types implantations), and in order to reduce short channel effects and to adjust the threshold voltage of the device, respectively.

Regarding claim 21, Singh et al. do not state that the step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate.
Boissonnet et al. teach the step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate.
Nishinohara teaches the step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate, in order to obtain proper doping distribution.

Regarding claim 23, Singh et al. do teach the notched spacer comprising silicon nitride .
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a notched spacer comprising silicon nitride in prior art's device in order to provide better protection for the device.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al., Boissonnet et al. and Nishinohara, as applied to claim 16 above, and further in view of Chen et al. (6,610,571).
Singh et al., Boissonnet et al. and Nishinohara teach substantially the entire claimed structure, as applied to claim 16 above, except teaching the method of forming the notched spacer.

Chen et al. teach in figures 2-4 and related text a method of forming a notched spacer comprises forming a first layer 50 and a second layer 52, forming a mask out of the second layer on the first layer, wherein an upper portion of the first layer 50 alongside an upper portion of at least one sidewall of the gate electrode 14 is covered by the mask(see figure 3), and wherein a lower portion of the first layer 50 at the surface of the substrate and a lower portion of the at least one sidewall of the gate electrode is not covered by the mask, isotropically etching the first layer such that the lower portion of the first layer is partially removed, and removing the mask (the portion of layer 52, as depicted in figure 4, which was used as a mask).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's notched spacer by forming a first layer and a second layer, forming a mask out of the second layer on the first layer, wherein an upper portion of the first layer alongside an upper portion of at least one sidewall of the gate electrode is covered by the mask, and wherein a lower portion of the first layer at the surface of the substrate and a lower portion of the at least one sidewall of the gate electrode is not covered by the mask, isotropically etching the first layer such that the lower portion of the first layer is partially removed, and removing the mask, in order to simplify the processing steps of making the device by using a conventional method.

Regarding claim 19, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a mask formed of silicon dioxide in prior art's

device in order to simplify the processing steps of making the device by using conventional isolating material, of which official notice is taken.

Claims 16, 21-24 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakai et al. ("A 100 nm CMOS Technology with "Sidewall-Notched" 40 nm Transistors and SiC-Capped Cu/VLK Interconnects for High Performance Microprocessor Applications", 2002 Symposium on VLSI Tecnnology Digest of Technical Papers (2002) pp. 66-67) in view of Boissonnet et al. and Nishinohara. Regarding claims 16 and 22, Nakai et al. teach in figures 1 and 3 and related text a method of forming a semiconductor device, the method comprising:

forming a gate electrode having sidewalls on a region in a substrate, the region in the substrate having a first conductivity type;

forming a notched spacer alongside the gate electrode sidewalls, the notched spacer having a first thickness in an upper portion and a second less thickness less than the first thickness in a lower portion adjacent to a surface of the substrate thereby forming a notch in the lower portion of the notched spacer, the notched spacer comprising a single homogenous silicon dioxide layer;

Nakai et al. do not teach performing a first ion implant at an oblique angle to the substrate so as to implant ions beneath the gate electrode wherein the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type.

Boissonnet et al. teach in figures 12 and 13 and related text performing a first ion implant 22 at an oblique angle to the substrate so as to implant ions beneath the gate electrode 51 wherein the gate electrode 51 and the notched spacer 181 act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type.

Nishinohara teach in figures 8 and 9 and related text (column 8, lines 52-63) performing a first ion implant at an oblique angle to the substrate so as to implant ions (halo region) beneath the gate electrode 4 wherein the gate electrode 4 and the spacer 20a act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to perform a first ion implant at an oblique angle to the substrate so as to implant ions beneath the gate electrode wherein the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type in Nakai et al.'s device in order to operate the device in its intended use by simplifying the processing steps of making the device by using the device in a CMOS application (which requires first and second conductivity types implantations), and in order to reduce short channel effects and to adjust the threshold voltage of the device, respectively.

Regarding claims 24, Nakai et al. teach in figures 1 and 3 and related text a method of forming a semiconductor device, the method comprising:

forming a gate electrode over a region on a substrate, the region of the substrate having a first conductivity type (inherently therein);

forming a first layer having a first thickness over the substrate and the gate electrode;

forming a second layer over the first layer;

removing a portion of the second layer such that a spacer mask is formed on the first layer on a sidewall of the gate electrode, wherein an upper portion of the first layer remains remaining covered by the spacer mask, and wherein a lower portion of the first layer extending along a surface of the substrate and extending up a lower sidewall portion of the sidewall of the gate electrode is exposed;

etching the first layer to form a notched spacer in the first layer, wherein the spacer mask acts as a mask, and wherein the etching partially removes the lower portion of the first layer thereby forming a notch in the notched spacer such that the notched spacer has a second thickness in a direction substantially orthogonal to the sidewall of the gate electrode along the surface of the substrate that is less than the first thickness;

removing the spacer mask (see figure 3);

Nakai et al. do not state isotropicaliy etching and performing a first ion implant after the spacer mask has been removed, the first ion implant using ions of the first conductivity type implanted at an oblique angle to the surface of the substrate and implanting ions

beneath the gate electrode; and performing one or more second ion implants using ions of a second conductivity type.

Boissonnet et al. teach in figures 12 and 13 and related text performing a first ion implant 22 at an oblique angle to the substrate so as to implant ions beneath the gate electrode 51 wherein the gate electrode 51 and the notched spacer 181 act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type.

Nishinohara teach in figures 8 and 9 and related text (column 8, lines 52-63) performing a first ion implant at an oblique angle to the substrate so as to implant ions (halo region) beneath the gate electrode 4 wherein the gate electrode 4 and the notched spacer 20a act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to isotropicaliy etching and performing a first ion implant after the spacer mask has been removed, the first ion implant using ions of the first conductivity type implanted at an oblique angle to the surface of the substrate and implanting ions beneath the gate electrode; and performing one or more second ion implants using ions of a second conductivity type, in Schuegraf et al.'s device in order to operate the device in its intended use by simplifying the processing steps of making the device by using conventional processing steps, in order to use the device in a CMOS application (which

requires first and second conductivity types implantations), and in order to reduce short channel effects and to adjust the threshold voltage of the device, respectively.

Regarding claims 21 and 26, Nakai et al. do not state that the step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate. Boissonnet et al. teach the step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate.
Nishinohara teaches the step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's step of performing one or more second ion implants is performed at an angle normal to a surface of the substrate, in order to obtain proper doping distribution.

Regarding claims 22-23, 27 and 28, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first layer and a mask formed of silicon dioxide and a second layer and a mask formed of silicon nitride in prior art's device in order to simplify the processing steps of making the device by using conventional etching stop material and isolating material, of which official notice is taken.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakai et al., Boissonnet et al. and Nishinohara, as applied to claim 16 above, and further in view of Chen et al. (6,610,571).

Regarding claim 17, Nakai et al., Boissonnet et al. and Nishinohara teach substantially the entire claimed structure, as applied to claim 16 above, except teaching the method of forming the notched spacer.

Chen et al. teach in figures 2-4 and related text a method of forming a notched spacer comprises forming a first layer 50 and a second layer 52, forming a mask out of the second layer on the first layer, wherein an upper portion of the first layer 50 alongside an upper portion of at least one sidewall of the gate electrode 14 is covered by the mask(see figure 3), and wherein a lower portion of the first layer 50 at the surface of the substrate and a lower portion of the at least one sidewall of the gate electrode is not covered by the mask, isotropically etching the first layer such that the lower portion of the first layer is partially removed, and removing the mask (the portion of layer 52, as depicted in figure 4, which was used as a mask).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's notched spacer by forming a first layer and a second layer, forming a mask out of the second layer on the first layer, wherein an upper portion of the first layer alongside an upper portion of at least one sidewall of the gate electrode is covered by the mask, and wherein a lower portion of the first layer at the surface of the substrate and a lower portion of the at least one sidewall of the gate electrode is not covered by the mask, isotropically etching the first layer such that the

lower portion of the first layer is partially removed, and removing the mask, in order to simplify the processing steps of making the device by using a conventional method.

Regarding claim 19, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a mask formed of silicon dioxide in prior art's device in order to simplify the processing steps of making the device by using conventional isolating material, of which official notice is taken.

***Response to Arguments***

1. Applicant argues that the passage "[i]n other situations, a portion of the first dielectric layer 126 may remain on the side of the gate electrode 122." illustrates that the Applicants had possession of the example depicted in Figure 1j, where "a portion of the first dielectric layer 126 may remain on the side of the gate electrode 122.".

The above passage does not support the structure depicted in figure 1j, because leaving a portion of the first dielectric layer on the side of the gate electrode 122 does not mean that the spacer MUST have a second thickness in a direction substantially orthogonal to the sidewall of the gate electrode along the surface of the substrate that is less than the first thickness, as depicted in figure 1j.

2. Applicant argues that the hypothetical structure described in the final office action, and illustrated on page 10 of the present response, would not accomplish the desired functions of when "a portion of the first dielectric layer 126 may remain on the side of the gate electrode 122" to further evidence that the hypothetical is not a correct interpretation of the specification. "The specification states in reference to when "a portion of the first dielectric layer 126 may remain" that ~[t]his may be desirable, for example, when it is preferred.., to protect the gate electrode 122 or gate dielectric 120 from damage during the etching process or other processes." In the above hypothetical, the gate dielectric 120, and in some situations a portion of the gate electrode, is exposed, and thus, would not be protected during etching or other processes. However, the example depicted in Figure 1j would obtain this desired effect because neither the gate electrode 122 nor the gate dielectric 120 is exposed, and thus, they are both protected. Accordingly, the Examiner's hypothetical is an incorrect interpretation of the specification, and a person having ordinary skill in the art would understand the recited passage to describe the embodiment depicted in Figure 1j".

Paragraph [0010] of the disclosure recites "In another embodiment of the present invention, a semiconductor device is provided having a notched spacer alongside a gate electrode. The notched spacer is formed alongside the gate electrode such that a portion of the notched spacer is completely or partially removed along the corner formed between the surface of the substrate and the gate electrode sidewall. A second spacer is formed alongside the notched spacer". This embodiment cannot be combined with other embodiments recited in the specification. Although the specification recites in one

embodiment that the gate electrode or gate dielectric should be protected from damage during the etching process or other processes, this one embodiment should not be combined with the above embodiment.

Furthermore, in the embodiment of figure 1E, as originally filed, it is clear that the gate electrode or gate dielectric is NOT protected from damage during the etching process or other processes. If the gate electrode or gate dielectric must be protected from damage during the etching process or other processes, then this embodiment is also "an incorrect interpretation of the specification".

3. Applicant argues that since "Boissonnet teaches forming P-type wells 13 and 14 in a substrate 1. Boissonnet col. 2, lines 53-62; Figure 1 (P-type well 13 is labeled 12 in the figure). Boissonnet then teaches, with reference to Figure 12, that a second dopant 22 is implanted, that the implantation is oblique, and that the second dopant is arsenic or phosphorus. Boissonnet col. 4, lines 1-17. Arsenic and phosphorus are both well-known n-type ion dopants", then "the asserted "first ion implant 22" is of a different conductivity type than the region in the substrate 1 on which the gate 51 is formed", and thus "the asserted "first ion implant 22" does not "us[e] ions of the first conductivity type" wherein "the first conductivity type" refers to the conductivity type of the region in the substrate on which the gate electrode is formed".

Boissonnet was not cited to teach an artisan the conductivity types of the "first ion implant". Boissonnet et al. was cited to teach an artisan that a first ion implant can be formed at an oblique angle to the substrate so as to implant ions beneath the gate

electrode wherein the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type.

Clearly, an artisan will form the conductivity types of the semiconductor device such that the device is operational. An artisan will not form a device having conductivity types which will render the device inoperative.

4. Applicant argues that Boissonnet does not teach a "notched spacer" because "spacer 181 has a first thickness in an upper portion that not only does not have a second thickness less than the first thickness in a lower portion adjacent to the surface of the substrate, but has a second greater thickness in the lower portion".

A notched spacer is a spacer a recess in the surface thereof. A notched spacer is NOT a spacer which must have a first thickness in an upper portion and a second less thickness less than the first thickness in a lower portion adjacent to a surface of the substrate, as argued by applicant. Boissonnet teaches a spacer having a recess in the surface (the upper surface) thereof. Thus, Boissonnet teaches a notched spacer.

In any event, Boissonnet was not cited to teach an artisan the conductivity types of the "first ion implant". Boissonnet et al. was cited to teach an artisan that a first ion implant can be formed at an oblique angle to the substrate so as to implant ions beneath the gate electrode wherein the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity

type, and performing one or more second ion implants using ions of a second conductivity type.

5. Applicant argues that Nishinohara does not teach a "notched spacer" because "offset spacers 20a and 20b have a uniform thickness in an upper portion and in a lower portion adjacent to the surface of the substrate, and not "a first thickness in an upper portion and a second thickness less than the first thickness in a lower portion adjacent to a surface of the substrate".

Nishinohara was not cited to teach an artisan a "notched spacer". Nishinohara was cited to teach an artisan forming a first ion implant at an oblique angle to the substrate so as to implant ions beneath the gate electrode wherein the gate electrode and the spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity type, and performing one or more second ion implants using ions of a second conductivity type.

6. The rest of applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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